REMARKS

This Amendment is submitted in response to the final Office Action of April 21, 2005 (hereinafter "the Office Action") and the Advisory Action of July 19, 2005. Upon entry of this Amendment, claims 1-3, and 20-25 will be pending in this Application.

All references to the claims, except as noted, will be made with reference to the claim list above beginning on page 2. Unless the source document contains line numbers (e.g., issued U.S. patents) all citations herein containing line numbers will count every printed line, except the page header, but including section headings. References to "the Application" will be made to the substitute specification submitted November 17, 2003. If there is any confusion or questions regarding any aspect of this Amendment, the Examiner is invited to contact the undersigned.

Status of claims

Claims 1-3 and 19 stand rejected under 35 U.S.C. § 102(b) and claims 20 and 21 stand rejected under 35 U.S.C. § 103(a) based on newly-cited art. Applicants note with appreciation the withdrawal of previous objections and rejections under 35 U.S.C. §§ 112, 102, and 103.

Form 892

Applicants note that the Office Action cites a new reference, U.S. Patent 5,375,216 to Moyer et al., which is not of record or listed in a Form 892. So that the prior art reference appears on the face of the printed patent, Applicants respectfully request that the Examiner cite the new reference in an 892.

Amendment

The present Amendment makes several clarifications with respect to claims 1, 2, and 3, cancels claim 19 as not being necessary, and makes claim 20 depend from claim 1. In addition, new claims 22-25 are presented. Claim 1 is modified to define the backing register file as containing a plurality of registers, each of which are assigned an address. This language is consistent with the whole of the disclosed invention and is particularly supported by the paragraph beginning at line 7 on page 15 of the Application. Claim 2 is corrected to set forth that each execution unit is operably connected to only one, not each, of the plurality of register files as shown in Figure 3. Claim 3 is amended to improve clarity and readability.

New claims 22-25 are directed to the backing register file portion of the processor, which is set forth in claims 1-3, 20, and 21. This Amendment contains no new matter.

Claim Rejections -- 35 U.S.C. § 102(b)

Claims 1, 2, 3, and 19 stand rejected under 35 U.S.C. § 102(b) for being anticipated by U.S. Patent 5,375,216 to Moyer et al. (Moyer). Applicants respectfully traverse because each and every claim limitation is not disclosed by Moyer. With regard to claim 19, Applicants note that this claim is canceled by this Amendment.

For anticipation under 35 U.S.C. § 102(b), each and every claim element must be present or inherent in the cited reference. There are numerous distinctions between the invention as claimed in claims 1-3 and Moyer. What follows is a discussion of several differences; any one of which is sufficient to overcome the rejection under 35 U.S.C. § 102(b).

1. The term, "plurality of registers" in claim 1 distinguishes from a data cache

Claim 1 sets forth, inter alia, "a backing register file comprising a plurality of registers . . ." (claim 1, line 8). The Office Action identifies "Moyer column 5, lines 34-39); column 6, lines 50-64; Figure 1, element 24; Figure 5; Figure 6; and Figure 7" (Office Action, page 3, lines 1-3) as reading on the backing register file containing a plurality of registers. Applicants respectfully disagree.

During examination, the Office is obliged to give claim elements the broadest *reasonable* interpretation to claim elements, and this interpretation must be consistent with the interpretation that those skilled in the art would reach. The "broadest reasonable interpretation" should be the "plain meaning" or "ordinary and customary interpretation" of the term, which may be evidenced by a variety of sources, including: the claims themselves, dictionaries and treatises, the written description, the drawings, and the prosecution history. See MPEP 2111.

In the present Application, the phrase, "plurality of registers," would *not* have been understood by persons having ordinary skill in the art as reading on the memory data cache storage locations of Moyer. Unlike registers, data cache storage locations are not directly accessible. Cache memory is invisible to the operation of the software. Even in the case of Moyer, wherein the instruction set is augmented to allow "touch load" "flush load" and other instructions which affect the cache (Moyer, col. 4, lines 6-8; col. 4, lines 35-43), the data

stored is only incidentally accessed when it happens to contain a copy of data stored in a particular location in main memory that is accessed by the physical address of the memory (col. 11, line 67 to col. 12, line 3; col. 16, lines 20-35 and 44-48).

Referring to Figure 3 in Moyer, a virtual address (referred to by Moyer as "effective address") is received by data cache memory management unit (MMU) 58 and translated into a physical address that is passed to the data tag array 56 (Moyer, col. 11, lines 11-15; col. 13, lines 14-16). The data tag array stores physical addresses and meta data corresponding to values stored in the data cache 54 (col. 11, line 67 to col. 12, line 3).

Since the data cache storage locations are not registers, the program cannot assign a particular value to a particular location in the cache. Depending on the associativity of the cache, which is not specified by Moyer, the value may depend on the physical address of the location it is stored in main memory, or it may be completely out of the control of the software as to where the value is stored in the cache. Because the cache stores a copy of a small subset of the main memory, each storage location in the cache can correspond to numerous possible storage locations in the main memory and therefore has no assigned address. On the other hand, registers are typically directly accessible via a unique address.

Because the term "register" defines over the data cache of Moyer, Applicants respectfully submit that claim 1 is not anticipated by Moyer and is therefore allowable. Furthermore, since claims 2, 3, and 19-21 further limit the invention set forth in claim 1, they are allowable for at least the same reasons as claim 1.

2. The Prior Art does not teach a backing register file as set forth in claim 1.

Claim 1 further defines "backing register file" as:

> "a backing register file comprising a plurality of registers, . . . said backing register file . . . in at least one mode, is always visible outside the processor and available to the programs at any privilege level such that each of the plurality of registers is accessible at random using a uniquely assigned address"

(claim 1, lines 8-13).

Moyer discloses a data cache for storing copies of data in the main memory for fast retrieval (col. 1, lines 12-14). As mentioned above, the memory locations in Moyer's data cache are not directly accessible via an assigned address. Each location stores a copy of data for one of a plurality of physical addresses, depending on the associativity of the data cache.

Thus, each storage location in the cache can correspond to numerous possible storage locations in the main memory and therefore has no assigned address as set forth in claim 1.

Thus, since Moyer does not provide a plurality of registers that "can [each] be accessed at random using an address uniquely assigned to that register" (claim 1, lines 16-18), claim 1 is not anticipated by Moyer. Applicants therefore respectfully submit that claim 1 is allowable over the prior art of record. Furthermore, since claims 2, 3, 20, and 21 depend from claim 1, applicants submit that they are allowable for at least the same reasons as claim 1.

3. The prior art does not teach a backing register having features of claim 2.

Claim 2 sets forth that the backing register file "allows transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file . . ." (claim 2, lines 4-8). The Office Action cites Moyer column 6, lines 50-64; Figure 1; Figure 5; Figure 6; and Figure 7 as reading on this feature (Office Action, page 3, lines 20-21). Applicants have carefully reviewed the indicated portions of Moyer but do not see any suggestion of moving data from any designated location in any designated register file of Moyer to any designated location of the data cache. As mentioned previously, the data cache is not addressable memory and therefore does not support placing a value in a designated location. The addresses mentioned by Moyer are either "effective addresses" which is Moyer's terminology for virtual addresses, or physical addresses, and these do not specify a location in the cache, but a location in main memory. Depending on the associativity of the cache, the possible locations are either restricted depending on the location of the data in the main memory, or out of the control of the software.

Applicants therefore respectfully submit that Moyer does not teach each and every limitation set forth in claim 2 and therefore claim 2 is not anticipated by Moyer, and therefore, claim 2 is allowable over the prior art of record.

Claim Rejections -- 35 U.S.C. § 103(a)

Claims 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Moyer in view of the Wikipedia article, "Register Window," hereinafter referred to as "Wikipedia." (Office Action, page 4, lines 18-20). Specifically, the Office Action states that "it would have been obvious . . . to incorporate the register windows of Wikipedia in the

device of Moyer to improve performance" (page 5, lines 13-15). Applicants respectfully disagree.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Second, there must be some reasonable expectation of success. [...] The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP 2143. The Office Action does not identify any motivation in the prior art for combining Moyer with Wikipedia, stating only that,

> "[a] person of ordinary skill in the art at the time the invention was made would have recognized that register windowing is reduces the amount of time necessary to save data to memory when a procedure call is present, since it does not require the data in the register to be moved from the registers to memory, thereby improving performance"

(Office Action, page 5, lines 9-13).

Applicants agree that register windowing can improve performance of a computing system, that the memory cache of Moyer can improve performance of a computing system, and it was known that improved performance is desirable. However, Applicants do not see any motivation in the prior art for making the data cache of Moyer ***mimic*** register windowing functionality as set forth in claim 20 as it relates to the disclosed backing register file. The Office may not rely on references that teach that the various aspects of the claimed invention were individually known in the art to establish a prima facie case of obviousness without some objective reason to combine the teachings. The prior art shows that it may have been obvious to provide a processor with both register windowing capability and a data cache, but there is no suggestion or teaching to modify the data cache so that it mimics register windowing as set forth in claim 20.

Furthermore, since the disclosed backing register file contains a plurality of registers that are addressable and randomly accessible, causing the backing register file to mimic register windowing functionality would be well within the abilities of the ordinary practitioner that has access to the present disclosure. However, the data cache disclosed by Moyer does not have the capability of being used for register windowing since it can only be used to store a subset of data from the main memory. Since a data cache cannot operate in the manner proposed in the Office Action, there could not have been any reasonable expectation of success.

Since there was no motivation to modify the prior art references as proposed in the Office Action, and because there was no reasonable expectation of success to make the combination as proposed, Applicants respectfully submit that claim 20 is patentable under 35 U.S.C. § 103(a) over Moyer and Wikipedia. Applicant therefore respectfully submits that claim 20 is allowable under 35 U.S.C. § 103(a). Furthermore, since claim 21 depends from claim 20 Applicants submit that claim 21 is allowable for at least the same reasons as claim 20.

For the reasons listed above, Applicants respectfully submit that this application is now in condition for allowance and earnestly request the same. Should any issue remain outstanding, Applicants invite the Examiner to contact the undersigned so that any remaining issues can be quickly resolved. Likewise, if the Examiner has any questions or concerns regarding the present Amendment, the Examiner is invited to contact the undersigned at (408) 774-6933.

If any fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP298). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Leonard Heyman, Esq.
Reg. No. 40, 418

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
Telephone: (408) 749-6900
Facsimile: (408) 749-6901
Customer Number 32291